3D MEMS wafer level packaging exemplified by RF characterized TSVs & TGVs and integration of bonding processes

Jessica Liljeholm, Peter Ågren, Niklas Svedin, Zargham Baghchehsaraei, Thorbjörn Ebefors.

SILEX Microsystems AB; Bruttovägen 1, Box 595, Järfälla, SE-175 26, SWEDEN

One of the main challenges in 3D packaging technology of RF devices is to combine excellent electrical RF performance together with a successful integration of the packaging process with the RF devices. In this abstract, Silex Microsystems, the world's largest pure play MEMS foundry, presents our most recent results on 3D integration using wafer level bonding in combination with Through Silicon Via (TSV) and Through Glass Via (TGV) capping substrates with RF devices.

In the full paper we will benchmark various tested methods of defining via holes in silicon and glass using both etching and laser drilling including cost of ownership (COO) analysis. As a complement to Silex' well established silicon via technology we present various metallization schemes including thick electroplating of gold and copper via fill for best possible RF performance. The TSVs and TGVs are integrated into the wafer level RF package using metal bonding, such as thermo compression and eutectic bonding, forming low Ohmic wafer-to-wafer interconnect as well as hermetic sealing.

Successful integration of both TSV and TGV capping substrates have been verified using different coplanar waveguides (CPWs) test vehicles. The TSV and TGV capping substrates have been electrically characterized showing low insertion losses below 0.04dB at 5GHz. Further details will be disclosed in the conference presentation and the full paper.

Portions of this work were accomplished under support by the European Union [ENIAC JU grants], National Swedish funding is provided in part by VINNOVA, the Swedish Governmental Agency for Innovation Systems.